VI-3 SERIES STACKED VARACTORS FOR HIGH POWER, HIGH FREQUENCY APPLICATIONS

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INTRODUCTION

In 1965 Irwin and Swan[1] of BTL, and also Varian Associates[2] in February 1967, demonstrated that series-connecting of two or more varactors enables one to obtain on the order of five times increase in power handling capability of a varactor multiplier, compared to a single element device. They showed that the total BV_R is the sum of the BV_R's of the individual devices, the C_j is the series sum of the capacitances, and the f_c is approximately equal to that of the individual chips. If N devices are series-connected and if the capacitance of the assembly is to be kept constant, the individual chip can have a value of capacitance approximately N times as large as that of the series-connected assembly. This can provide a thermal resistance decreased by about the same ratio, provided adequate heat sinking is provided.

The author of the above papers partially demonstrated the possible advantages of series connection of varactors by soldering two, three or four packaged varactors together, one on top of the other. They did not realize the full power dissipation capability of series-connected varactors, because, in their assemblies, only the bottom varactor which was attached to the heat sink, was efficiently cooled.

The approach described in this paper consists of bonding two or more silicon varactor chips onto metalized lands on a beryllia substrate. The substrate is then soldered onto a standard varactor housing. With this approach, all of the silicon chips are located close to the heat sink on a high thermal conductivity insulator. Beryllia was chosen over alumina because the thermal conductivity of beryllia is 8 times that of alumina and is greater than one-half that of pure copper.

The construction details of a four chip assembly are seen in Figure 1. The first structure tried utalizes gold wire thermal compression bonding for top contacts and eutectic alloying for back contacts. A cross section of a three chip assembly is seen in Figure 2. Excellent bonding is seen between the silicon chips and the beryllia, as well as between the beryllia and the housing.

STATIC DATA

Table I presents data which illustrates the advantages of series-connecting varactors. The assemblies were fabricated in cartridge packages with one, two and three silicon chips (all from one wafer) bonded onto beryllia substrates.

TABLE I – SERIES INTEGRATED VARACTORS WITH 1, 2, AND 3 CHIPS (All From One Wafer)

ASSEMBLY	No. Samples Tested	BV_R 10μa Volts	C_j 6v pf	fco 6v GHz	θ* °C/W	Max** Diss. 25°C Watt
One Chip with BeO Substrate	4	45	0.23	70	45	3.3
Two Chips with BeO Substrate	5	90	0.15	85	25	6.0
Three Chips with BeO Substrate	2	120	0.095	80	16.5	9.1
One Chip with no BeO Substrate	3	45	0.23	70	53	2.8

*Thermal Resistance was measured per MIL-STD-750 Method 4081.

**The Maximum dissipation is based on a maximum junction temperature = 175 C.

In comparing 1, 2 and 3 chip assemblies it is obvious that, as N chips are added in series, the BV_R increases approximately by a factor of N, the C_j decreases by approximately C/N and the fco, within measurement uncertainly, does not decrease. Of special significance is the nearly linear decrease in thermal resistance with N, and the corresponding increase in maximum dissipation capability. In addition, because BV_R is increased by a factor of N_2 the power handling capability is theoretically increased by a factor of N^2.

Another test demonstrated in Table I is a comparison of one chip in a package with and without a beryllia substrate. It is expected that the beryllia should not introduce appreciable thermal resistance. The data implies an unanticipated improvement in θ which is tentatively explained as being due to process variables.

To make devices for specific applications it is desirable to design chips, which are to be used as building blocks,according to the electrical characteristics desired of the final assembly. This approach is illustrated in Table II where BV_R and C_j were maintained at specific levels by choosing chips for building blocks which have lower BV_R (permitting higher fco) and higher C_j. Here the integrated assembly duplicates the desired commercial equivalent device, with the advantage that the power dissipation capability is considerably improved.

TABLE II – SERIES INTEGRATION TO MAINTAIN CONSTANT C_j AND BV_R

Philco Part Number for Single Chip	BV_R 10μa Volts	C_j 6v pf	fco 6v GHz	θ °C/W	Max. Diss. 25°C Watt
L4854H	90	1.9	60	30	5
2 Chip Equivalent	90	1.7	65	15	10
L4831K	40	0.25	90	55	2.6
3 Chip Equivalent	110	0.25	130	20	7.5
Building Block used for 2 Chip Assembly	40	3.0	65	30	5

PARASITICS

It is recognized that the structure used in these preliminary samples will suffer more parasitics than single chip devices. Additional inductance is encountered due to the two or three lengths of wire in the inter-connections. Excess shunt capacitance is encountered because of the location of the metalized lands with respect to the base of the package. These parasitics result in parallel resonances at frequencies that are lower than those encountered with single chip constructions. In future models the parasitics will be reduced by any of several techniques that are available.

CIRCUIT EVALUATION

Circuit evaluation was obtained when series-integration was employed in varactors for the last two high frequency tripler stages of a solid-state Ku-band-power source, designed to generate >1 watt at 13.3 GHz. In the S-band tripler section of the multiplier, the diode consisted of a two-chip assembly in a standard pill prong package, and it was driven by 8 W at 1.5 GHz input. In the last stage, which is a tripler from 4.5 GHz to 13.5 GHz, another two-chip assembly in a pill prong package was used. It was driven by the output from the stage described above.

In both of the applications, the devices performed well and, because of the low thermal resistance the junction temperature was conservative.

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1. J.C. Irwin and C.B. Swan "A Composite Varactor for Simultaneous High Power and High Efficiency Harmonic Generator", IEEE Transactions on Electron Devices Vol. ED-13 No. 5 May 1966 p. 466-471.
2. Microwaves February 1966, Cover Feature pp 96.

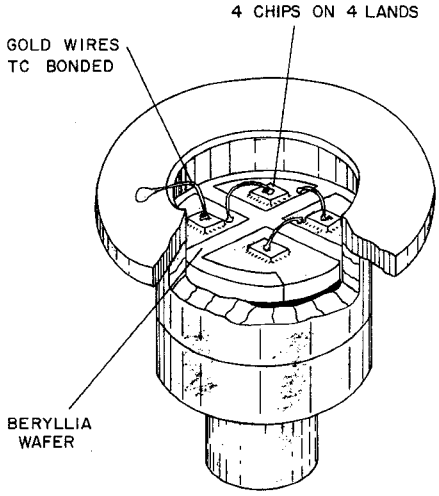

FIG. 1 - Four Chip Series Connected Varactor

FIG. 2 - Cross-Section of a Triple Chip Series Connected Varactor